1. A variable length decoder for decoding a stream of compressed video data, wherein the stream includes a plurality of variable length encoded data representing image areas of transmitted frames, comprising:

a memory for storing variable length encoded data;

a command decode and execution circuit coupled to the memory for receiving selected variable length encoded data from the memory;

a sequencer coupled to the command decode and execution circuit for providing commands to the command decode and execution circuit to convert the variable length encoded data into corresponding decoded values; and

a master controller coupled to the command decode and execution circuit for providing commands to the command decode and execution circuit independently of the sequencer to control decoding operation of the command decode and execution circuit.

2. The variable length decoder of claim 1 wherein the sequencer includes memory for storing a plurality of instructions and an instruction decode and control circuit coupled to the instruction memory for decoding instructions from the memory and providing commands to the command decode and execution circuit to convert the variable length encoded data into corresponding decoded values.

3. The variable length decoder of claim 1 further comprising a plurality of command instruction registers coupled to the sequencer and the master controller, wherein the sequencer and master controller are operable to read and write contents of the command instruction registers.

4. The variable length decoder of claim 3 wherein the command instruction registers are associated with the instructions provided to the command decode and execution circuit.

5. The variable length decoder of claim 1 further comprising a variable length table decoder coupled to the command decode and execution circuit for receiving variable length encoded data and provided a corresponding decoded value to the command decode and execution circuit.

6. The variable length decoder of claim 1 wherein the command decode and execution circuit is operable to decode variable length encoded data conforming to an MPEG syntax.

7. The variable length decoder of claim 6 wherein the command decode and execution circuit is operable to decode the variable length encoded data into DCT coefficient symbols each including a run-length value and an amplitude level value.

8. The variable length decoder of claim 7 further comprising a first-in first-out memory and decoder coupled to the command decode and execution circuit for storing the DCT coefficient symbols as compressed run-length and amplitude level pairs.

9. The variable length decoder of claim 8 further comprising an inverse DCT transform circuit coupled to the first-in first-out memory and decoder, wherein the first-in first-out memory and decoder is operable to decompress the run-length and amplitude level pairs into DCT coefficients for use by the DCT transform circuit in reconstructing image data of the transmitted frames.

10. The variable length decoder of claim 6 wherein the command decode and execution circuit is operable to decode the variable length encoded data into motion vector values.

11. The variable length decoder of claim 10 further comprising a first-in first-out memory coupled to the command decode and execution circuit for storing the motion vector values.

12. The variable length decoder of claim 11 further comprising a motion compensation circuit coupled to the first-in first-out memory, wherein the first-in first-out memory is operable to provide the motion vector values to the motion compensation circuit in reconstructing image data of the transmitted frames.

13. A variable length table decoder for decoding compressed video data using variable length code tables, wherein the compressed video data includes variable length encoded data representing an image area of a transmitted frame, comprising:

a memory for storing variable length encoded data;

a pattern match circuit coupled to the memory for identifying a unique prefix pattern in the variable length encoded data;

variable length code table data including a decoded value associated with each of a plurality of variable length codes, wherein the variable length code table data comprises a plurality of subtable data circuits each associated with a unique prefix pattern in the variable length codes;

a datapath coupling the memory to each of the subtable data circuits for applying variable length encoded data to each of the subtable data circuits; and

control circuitry responsive to the pattern match circuit for obtaining a decoded value from the subtable data circuit associated with the unique prefix pattern in the variable length codes that matches the identified prefix pattern in the variable length encoded data, and additional data in the variable length codes after the unique prefix pattern that

matches additional data in the variable length encoded data after the identified prefix pattern.

14. The variable length table decoder of claim 13 wherein each of the variable length codes includes an associated code length, and wherein the control circuitry is responsive to the pattern match circuit for obtaining a code length from the subtable data circuit associated with the unique prefix pattern in the variable length codes that matches the identified prefix pattern in the variable length encoded data, and additional data in the variable length codes after the unique prefix pattern that matches additional data in the variable length encoded data after the identified prefix pattern.

15. The variable length table decoder of claim 14 further comprising a shifter circuit associated with the memory for applying a predetermined number of bits of the variable length encoded data from the memory to the pattern match circuit.

16. The variable length table decoder of claim 15 wherein the shifter circuit includes a plurality of selector circuits for selectively shifting the variable length encoded data in the memory.

17. The variable length table decoder of claim 16 wherein the plurality of selector circuits are arranged in a plurality of selector stages, wherein each selector stage is operable to shift the variable length encoded data in memory by a power of two or to provide no shift of the variable length encoded data.

18. The variable length table decoder of claim 17 wherein at least one of the selector stages includes fewer selector circuits than a preceding selector stage.

19. The variable length table decoder of claim 17 wherein each selector stage includes fewer selector circuits than its preceding selector stage.

20. The variable length table decoder of claim 16 wherein the shifter circuit is responsive to the last obtained code value for shifting the variable length encoded data in the memory by a number of bits equal to obtained code value.

21. A method for decoding a stream of compressed video data using variable length code tables, wherein the stream includes a plurality of variable length encoded data representing image areas of transmitted frames, comprising the steps of:

defining a variable length code table including a decoded value associated with each of a plurality of variable length codes;

defining a plurality of unique prefix patterns associated with the variable length codes,

defining a plurality of subtables, wherein each subtable is associated with one of the unique prefix patterns in the variable length codes and includes at least one decoded value that is associated with the unique prefix pattern and additional data in the variable length code after the unique prefix pattern;

identifying in the variable length encoded data one of the unique prefix patterns associated with the variable length codes; and

obtaining a decoded value from the subtable associated with the unique prefix pattern in the variable length codes that matches the identified prefix pattern in the variable length encoded data, and additional data in the variable length codes after the unique prefix pattern that matches additional data in the variable length encoded data after the identified prefix pattern.

22. The method of claim 21 further comprising the steps of:

associating a code length with each of the plurality of variable length codes; and

obtaining a code length associated with the variable length code having a prefix pattern that matches the identified prefix pattern in the variable length encoded data, and additional data after the prefix pattern that matches additional data in the variable length encoded data after the identified prefix pattern.

23. The method of claim 21, further comprising the steps of:

identifying in the variable length encoded data one of the unique prefix patterns associated with the variable length codes; and

simultaneously applying the additional data in the variable length encoded data to each of the plurality of subtables,

wherein a decoded value is obtained from the subtable associated with the unique prefix pattern in the variable length codes that matches the identified prefix pattern in the variable length encoded data, and additional data in the variable length codes after the unique prefix pattern that matches additional data in the variable length encoded data after the identified prefix pattern.